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09/888,105	06/22/2001	Michael Ruehle	2207/11839	7951

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EXAMINER	
PATEL, NIMESH G	

ART UNIT	PAPER NUMBER
2112	5

DATE MAILED: 01/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	09/888,105	RUEHLE, MICHAEL	
	Examiner	Art Unit	
	Nimesh G Patel	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-30 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-30 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 19 October 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to because Figure 3b, block 320 is written incorrectly. Block 320 of Figure 3b states triggering "Put Bus," which is defined in the specification as connecting the SDRAM bus to the FPGA. Thus, "between Host and FPGA" should be replaced with "between SDRAM and FPGA." A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 7, 8, 17, 18, 27, and 28 recite the limitation "the third device." There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 4-7, 9-11, 14-17, 19-21, 24-27, and 29-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Abraham et al.('616) hereinafter referred to as Abraham.

6. Regarding claim 1, Abraham discloses a system to initiate, by a host(Figure 1, 103), an event in a first device(Figure 1, 107), the system comprising: a signal line(Figure 1, 115) to communicate a plurality of data values between a host and one or more second devices(Figure 1, 105); and a tap line to communicate said plurality of data values between said signal line and said first device; wherein said event is initiated upon detection, by said first device, of a predetermined sequence of data values on the tap line(Column 5, Lines 17-23).

7. Regarding claim 4, Abraham discloses wherein the host is a processor(Figure 1, 103).

8. Regarding claim 5, Abraham discloses the first device is a logic device (Figure 1, 107).

9. Regarding claim 6, Abraham discloses the second device being a memory device (Figure 1, 105).

10. Regarding claim 7, Abraham discloses the third device being a memory device (Figure 1, 109).

11. Regarding claim 9, Abraham discloses the plurality of data values representing a memory location within the second memory device(Column 2, Lines 57-69).

12. Regarding claim 10, Abraham discloses the utilization of a data value provides a call to the represented memory location(Column 2, Lines 57-69).

13. Regarding claim 11, Abraham discloses initiating, by a host, an event in a first device comprising: communicating, by a signal line, a plurality of data values between a host and one or more second devices; communicating, by a tap line, said plurality of data values between said signal line and said first device; and initiating said event upon detection by said first device of a predetermined sequence of data values on the tap line(Figure 1, Column2, Lines 8-13).

14. Regarding claim 14, Abraham discloses wherein the host is a processor(Figure 1, 103).

15. Regarding claim 15, Abraham discloses the first device is a logic device (Figure 1, 107).

16. Regarding claim 16, Abraham discloses the second device being a memory device (Figure 1, 105).

17. Regarding claim 17, Abraham discloses the third device being a memory device (Figure 1, 109).

18. Regarding claim 19, Abraham discloses the plurality of data values representing a memory location within the second memory device(Column 2, Lines 57-69).

19. Regarding claim 20, Abraham discloses the utilization of a data value provides a call to the represented memory location(Column 2, Lines 57-69).

20. Regarding claim 21, Abraham discloses a processor to initiate, by a host, an event in a first device comprising: communicating, by a signal line, a plurality of data values between a host and one or more second devices; communicating, by a tap line, said plurality of data values between said signal line and said first device; and initiating

said event upon detection by said first device of a predetermined sequence of data values on the tap line(Figure 1, Column2, Lines 8-13).

21. Regarding claim 24, Abraham discloses wherein the host is a processor(Figure 1, 103).

22. Regarding claim 25, Abraham discloses the first device is a logic device (Figure 1, 107).

23. Regarding claim 26, Abraham discloses the second device being a memory device (Figure 1, 105).

24. Regarding claim 27, Abraham discloses the third device being a memory device (Figure 1, 109).

25. Regarding claim 29, Abraham discloses the plurality of data values representing a memory location within the second memory device(Column 2, Lines 57-69).

26. Regarding claim 30, Abraham discloses the utilization of a data value provides a call to the represented memory location(Column 2, Lines 57-69).

27. Claims 1-3, 11-13, and 21-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Nozuyama('359).

28. Regarding claim 1, Nozuyama discloses a system to initiate, by a host(Figure 1, 11), an event in a first device(Figure 1, 3 and 14 combined), the system comprising: a signal line(Figure 1, 21) to communicate a plurality of data values between a host and one or more second devices(Figure 1, 12); and a tap line to communicate said plurality of data values between said signal line and said first device; wherein said event is

initiated upon detection, by said first device, of a predetermined sequence of data values on the tap line(Column 2, Lines 20-25).

29. Regarding claim 2, Nozuyama discloses switching of the communication path between the first device and a third device(Figure1, 15) and a communication path between the signal line and the third device(Column 2, Lines 20-25).

30. Regarding claim 3, Nozuyama discloses switching of the communication path between the first device and a third device(Figure1, 15) and a communication path between the signal line and the third device(Column 2, Lines 20-25).

31. Regarding claim 11, Nozuyama discloses a system to initiate, by a host(Figure 1, 11), an event in a first device(Figure 1, 3 and 14 combined), the system comprising: a signal line(Figure 1, 21) to communicate a plurality of data values between a host and one or more second devices(Figure 1, 12); and a tap line to communicate said plurality of data values between said signal line and said first device; wherein said event is initiated upon detection, by said first device, of a predetermined sequence of data values on the tap line(Column 2, Lines 20-25).

32. Regarding claim 12, Nozuyama discloses switching of the communication path between the first device and a third device(Figure1, 15) and a communication path between the signal line and the third device(Column 2, Lines 20-25).

33. Regarding claim 13, Nozuyama discloses switching of the communication path between the first device and a third device(Figure1, 15) and a communication path between the signal line and the third device(Column 2, Lines 20-25).

34. Regarding claim 21, Nozuyama discloses a system to initiate, by a host(Figure 1, 11), an event in a first device(Figure 1, 3 and 14 combined), the system comprising: a signal line(Figure 1, 21) to communicate a plurality of data values between a host and one or more second devices(Figure 1, 12); and a tap line to communicate said plurality of data values between said signal line and said first device; wherein said event is initiated upon detection, by said first device, of a predetermined sequence of data values on the tap line(Column 2, Lines 20-25).

35. Regarding claim 22, Nozuyama discloses switching of the communication path between the first device and a third device(Figure1, 15) and a communication path between the signal line and the third device(Column 2, Lines 20-25).

36. Regarding claim 23, Nozuyama discloses switching of the communication path between the first device and a third device(Figure1, 15) and a communication path between the signal line and the third device(Column 2, Lines 20-25).

Claim Rejections - 35 USC § 103

37. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

38. Claims 8, 18, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abraham.

39. Regarding claim 8, Abraham discloses a host is a microprocessor chipset (Figure 1, 103), the first device is a Field Programmable Gate Array (FPGA)(Figure 1, 107; Column 2, Line 48), the second device being a memory device (Figure 1, 105), and the third device being a memory device (Figure 1, 109). Abraham does not specifically disclose the use of a Dual In-line Memory Module (DIMM) or a Synchronous Dynamic Random Access Memory (SDRAM). However, SDRAM is a form of memory that can run at higher clock speeds. Therefore it would have been obvious to use SDRAM in Abraham's invention since it would speed up memory accesses. Also, DIMMs have become an industry standard because it can be installed one at a time compared to SIMMs requirement of being installed in pairs. Therefore, it would have been obvious to use DIMMs in Abraham's invention. Thus claim 8 is rejected.

40. Regarding claim 18, Abraham discloses a host is a microprocessor chipset (Figure 1, 103), the first device is a Field Programmable Gate Array (FPGA)(Figure 1, 107; Column 2, Line 48), the second device being a memory device (Figure 1, 105), and the third device being a memory device (Figure 1, 109). Abraham does not specifically disclose the use of a Dual In-line Memory Module (DIMM) or a Synchronous Dynamic Random Access Memory (SDRAM). However, SDRAM is a form of memory that can run at higher clock speeds. Therefore it would have been obvious to use SDRAM in Abraham's invention since it would speed up memory accesses. Also, DIMMs have become an industry standard because it can be installed one at a time compared to SIMMs requirement of being installed in pairs. Therefore, it would have been obvious to use DIMMs in Abraham's invention. Thus claim 18 is rejected.

41. Regarding claim 28, Abraham discloses a host is a microprocessor chipset (Figure 1, 103), the first device is a Field Programmable Gate Array (FPGA)(Figure 1, 107; Column 2, Line 48), the second device being a memory device (Figure 1, 105), and the third device being a memory device (Figure 1, 109). Abraham does not specifically disclose the use of a Dual In-line Memory Module (DIMM) or a Synchronous Dynamic Random Access Memory (SDRAM). However, SDRAM is a form of memory that can run at higher clock speeds. Therefore it would have been obvious to use SDRAM in Abraham's invention since it would speed up memory accesses. Also, DIMMs have become an industry standard because it can be installed one at a time compared to SIMMs requirement of being installed in pairs. Therefore, it would have been obvious to use DIMMs in Abraham's invention. Thus claim 28 is rejected.

Conclusion

42. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Toujima et al.('654) discloses two devices connected to a switch that gives access to a DRAM .

Dent et al.('575) discloses a that couples memory address, memory data and memory control signals to the data memory alternatively from the control processor or the coprocessor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nimesh G Patel whose telephone number is 703-305-7583. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Nimesh G Patel
Examiner
Art Unit 2112

NGP
NP

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